ADM-SDEV-BASE/XCKU060
User Manual

Document Revision: 1.7
27th Apr 2021

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1 Introduction

The **ADM-SDEV-BASE/XCKU060** is the **base board** at the core of the ADA-SDEV-KIT and ADA-SDEV-KIT2 space FPGA development kits. These kits enable customers interested in space grade FPGAs to prototype their applications on a compatible XCKU060-1I device.

The ADA-SDEV-KIT2 contains an ADM-SDEV-BASE/XCKU060 rev 2 board, while the ADA-SDEV-KIT contains an ADM-SDEV-BASE/XCKU060 rev 1 board.

The differences between revisons are as follows:

- The FPGA core power supply on the rev 2 board was uprated to 36A, on the rev 1 board this supply is rated at 24A.
- The rev 2 revision board has user controlled LEDs, a feature not present on the rev 1 board.

Note:
Other than the differences listed above, rev 1 and rev 2 revision boards are functionally identical. Unless stated otherwise all sections of this user manual apply equally to both revisions.

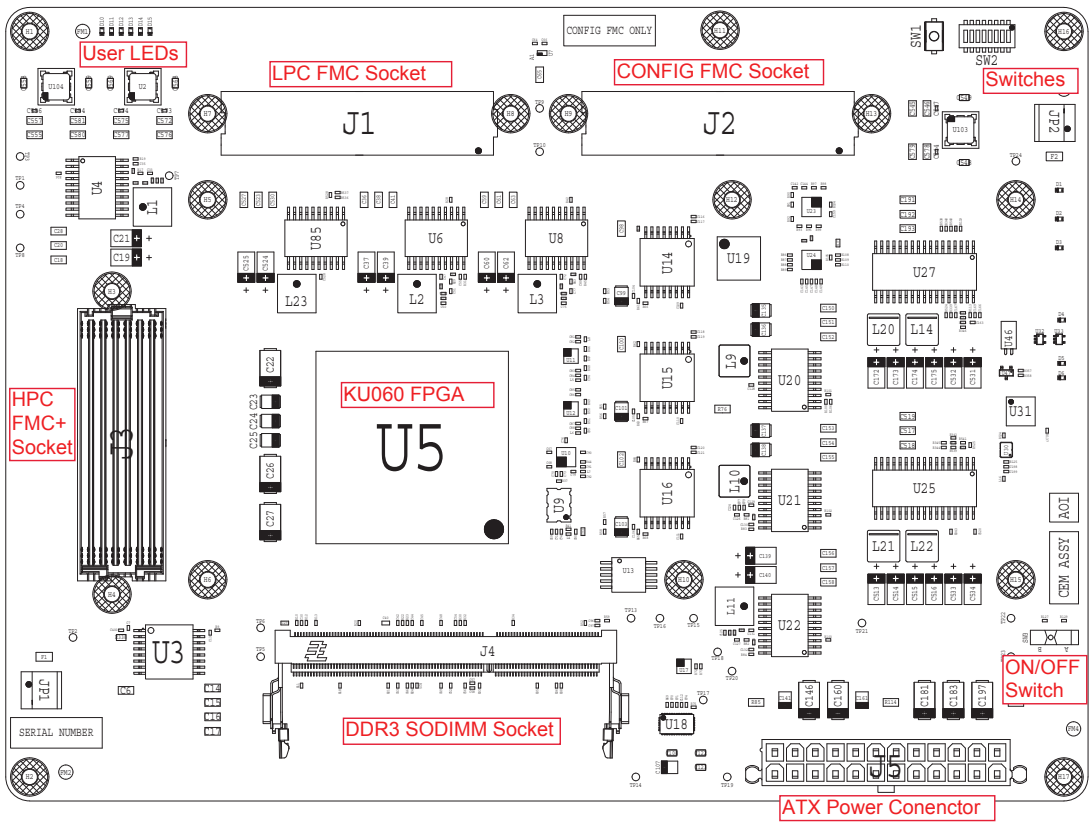

Figure 1 : ADM-SDEV-BASE/XCKU060 Top View (rev2 board shown)

1.1 Key Features

Key Features

- Custom Form Factor
- Modular design structure
- Powered via an external power supply
- Fitted with XCKU060-1FFVA1517I FPGA device as standard
- PCB footprint compatible with QRKU060-CNA1509 (Contact factory for details)
- 1x FMC+ HPC and 1x FMC LPC interfaces
- 1x FMC form factor configuration interface - clearly labelled **"XRTC-Standard Config-FMC Only"**
- DDR3 (with ECC) SODIMM connector to banks 66,67,68 for DDR3 support
- A JTAG header to allow Vivado Hardware Manager configuration and debug (requires ADM-SDEV-CFG1 or ADM-SDEV-CFG2 board)
- Programmable clock generation, controlled by I2C connected to the FMC config daughter base board and the FPGA
- Heatsink and Fan on top of KU060 FPGA

1.2 References & Specifications

ANSI/VITA 57.1	*FPGA Mezzanine Card (FMC) Standard*, July 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 57.4	*FPGA Mezzanine Card Plus(FMC+) Standard*, March 2016, VITA, Draft
ad-ug-0080	*ADA-SDEV-KIT Configuration Guide*, Nov 2018, Alpha-Data, v1.0
ad-ug-0081	*ADA-SDEV-KIT production Test Overview*, Sep 2019, Alpha-Data, v1.2
ad-ug-1361	*ADA-SDEV-CFG1 User Manual*, Nov 2018, Alpha-Data, v1.0
ad-ug-1423	*ADA-SDEV-CFG2 User Manual*, Apr 2021, Alpha-Data, v1.0

Table 1 : References

1.3 Environmental & Specifications

The operational temperature range of the ADA-SDEV-BASE board is outlined in Temperature Limits.

Note:
Note: The ADA-SDEV-KIT and ADA-SDEV-KIT2 are designed for use as development platforms only, are not space graded platforms and are not suitable for flight or radiation testing.

2 Installation

2.1 Software Installation

Please refer to the Alpha-Data support site for access to system monitoring utilities, documentation and FPGA reference designs.

2.2 Hardware Installation

2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2.2 Power Supply

The base board is designed to be powered via an external ATX power supply, connected via the standard 24-pin ATX12V 2.x power connector J5.

This external ATX power supply must be capable of providing a minimum of 20A (100W) on the +5V rail.

In its default configuration the ADA-SDEV-BASE board draws all of its power from the +5V rail.

Some ATX power supplies may not turn on without a minimum load on the +3.3V rail. Please contact the factory for further details. A list of power supplies that have been verified to work with the ADA-SDEV-KIT shall be maintained in document ad-ug-0081.

2.2.3 Cooling Requirements

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the exact current requirements for each power rail.

The board is supplied with an active air cooled heatsink.

The board features system monitoring that measures the board and FPGA temperature. It also includes a self-protection mechanism that will clear the target FPGA configuration if an over-temperature condition is detected.

See Section 3.5 for further details.

2.2.4 Configuration FMC Board

Prior to applying power the configuration FMC board (ADM-SDEV-CFG1, ADM-SDEV-CFG2 or similar) should be fitted into the Config FMC Socket (J2).

3 Functional Description

3.1 Overview

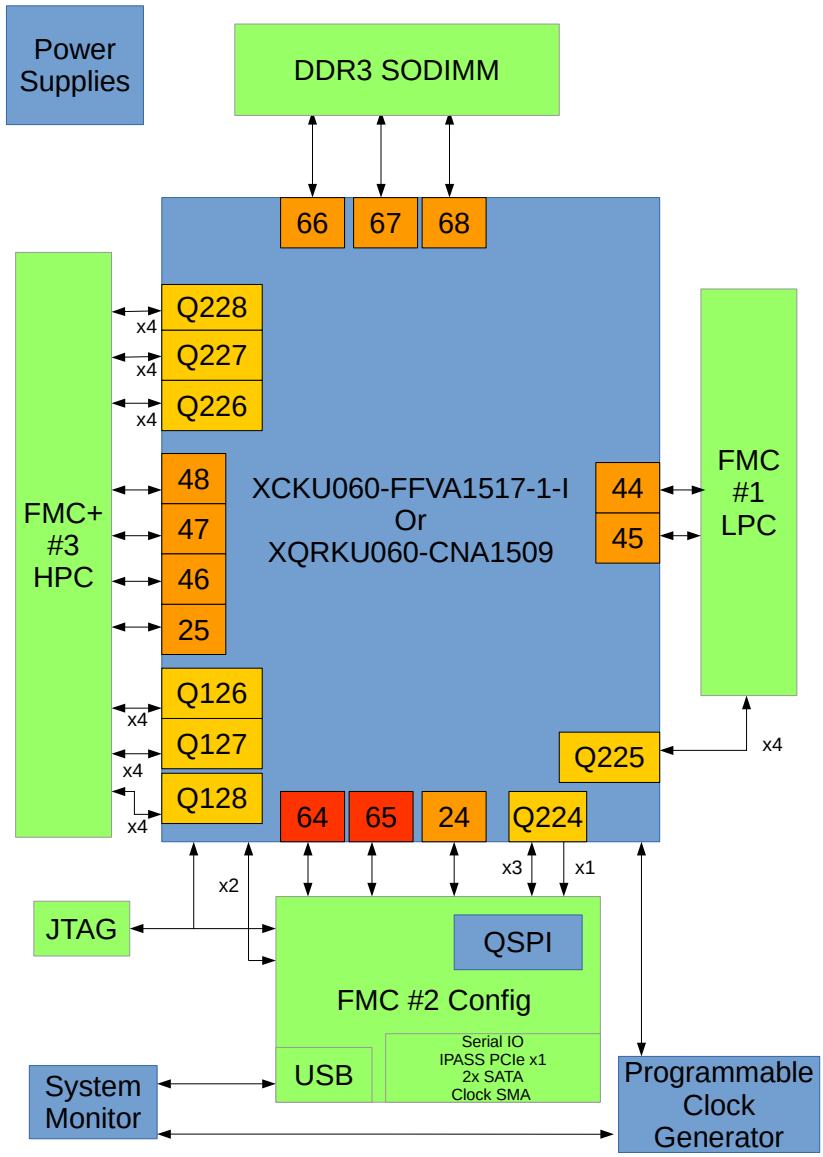

Figure 2 : ADM-SDEV-BASE/XCKU060 Block Diagram

3.1.1 Switch Definitions

There is a sliding switch situated on the bottom right corner of the board, plus a set of eight DIP switches and a push button switch placed on the top right corner of the board. Their functions are described in Switch Definitions.

Note:
All switches are OFF by default. *Factory Configuration* switch must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
SW1 (push button)	Reset	System Reset	Normal Operation
SW2-1	Reserved	-	Normal Operation
SW2-2	Reserved	-	Normal Operation
SW2-3	Config Disable	Configuration of the FPGA is disabled.	Normal Operation.
SW2-4	FPGA User 1 - FPGA Bank 64	User defined	User defined.
SW2-5	FPGA User 2 - FPGA Bank 24	User defined	User defined.
SW2-6	Reserved	-	Normal Operation
SW2-7	*Factory Configuration*	-	Normal Operation
SW2-8	Reserved	-	Normal Operation
SW3 (sliding)	POWER ON/ OFF	PSU ON (position A)	PSU OFF (position B)

Table 2 : Switch Definitions

3.1.2 Status LED Definitions

The position and description of the board status LEDs are shown in Status LED Locations:

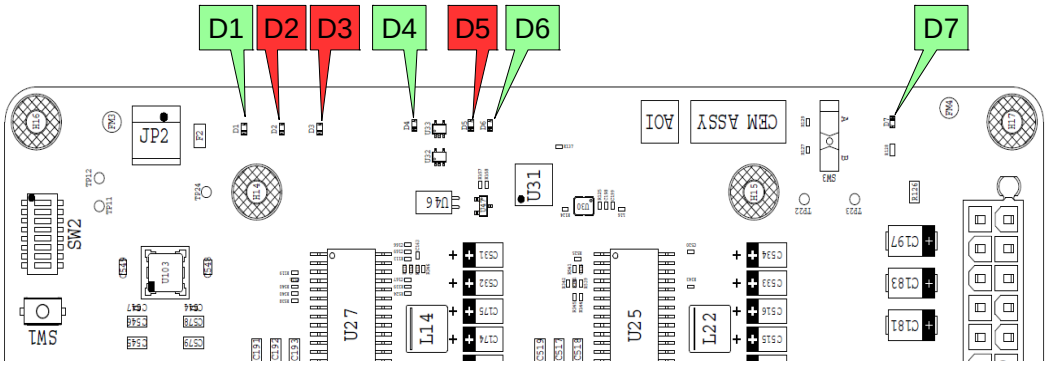

Figure 3 : Status LED Locations

Comp. Ref.	Function	ON State	Off State
D1(Green)	Status 0	See Status LED Definitions	
D2(Red)	Status 1	See Status LED Definitions	
D3(Red)	Internal Power Fault	Internal Power supply fault	Normal operation
D4(Green)	FPGA Done	FPGA is configured	FPGA is unconfigured
D5(Red)	Reserved for future use	-	-
D6(Green)	Reserved for future use	-	-
D7(Green)	ATX PSU Status	Normal operation	ATX PSU Off

Table 3 : Status LED Definitions

3.1.3 User LEDs - ADA-SDEV-KIT2 only

There are six user defined LEDs available on the board ,their positions are shown in User LED Locations:

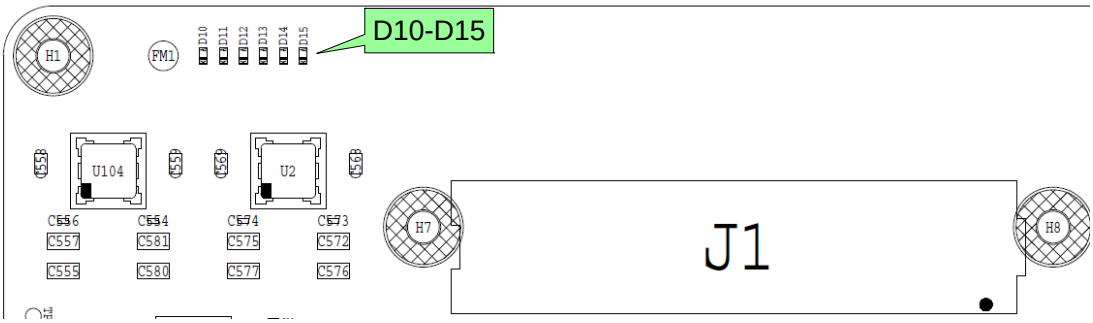

Figure 4 : User LED Locations

Comp. Ref.	Pin Loc
D10(Green)	AH31
D11(Green)	AH32
D12(Green)	AE30
D13(Green)	AF30
D14(Green)	AH28
D15(Green)	AJ28

Table 4 : User LED FPGA pin locations

Note:
User LEDs are only present on ADA-SDEV-KIT2 kits, i.e. base board pcb revision 2 onwards. No user LEDs are available on ADA-SDEV-KIT.

3.2 JTAG Interface

3.2.1 On-board Interface

A JTAG boundary scan chain can be accessed via a standard connector on the config FMC (J2). This allows the connection of the Xilinx JTAG cable for FPGA debug using the Xilinx toolchain.

The JTAG chain starts on the config FMC board and passes through the FPGA, the LPC FMC (J1) (if fitted) and the FMC+ (J3) (if fitted).

The scan chain is shown in JTAG Boundary Scan Chain:

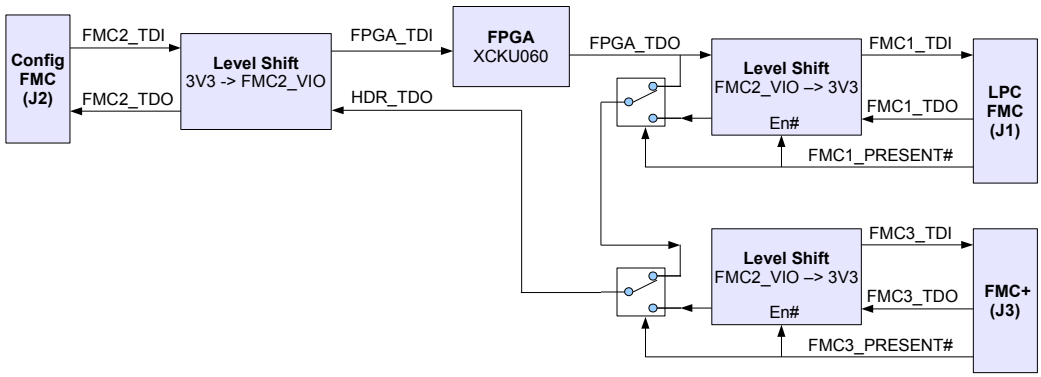

Figure 5 : JTAG Boundary Scan Chain

At each stage the clock signal on this JTAG interface (TCK) has a parallel termination (49.9Ω + 22pF to ground) located at the far end of the line.

3.2.2 JTAG Voltages

The Vcc supply provided to the JTAG cable on the config FMC is +3.3V and is protected by a poly fuse rated at 375mA.

The JTAG signals on all of the FMC boards use 3.3V signals and are connected through level translators to the ADM-SDEV-BASE board scan chain.

The voltage level of the JTAG chain on the ADM-SDEV-BASE board is set to the config FMC adjustable voltage FMC2_VIO.

3.3 Clocks

The **ADA-SDEV-BASE** board provides a wide variety of clocking options. In addition to the and clocks routed from the FMC connectors, the board has 2 user-programmable clock generators. These clocks can be combined with the FPGA's internal PLLs to suit a wide variety of communication protocols.

A complete overview of the clock routing on the **ADA-SDEV-BASE** is given in Clocks. A description of each clock follows.

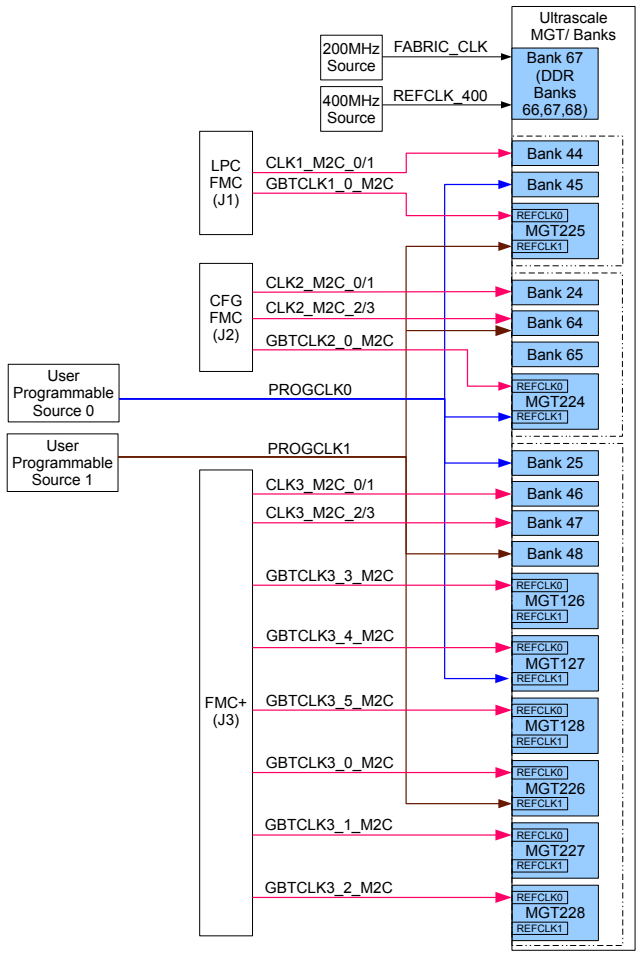

Figure 6 : Clocks

3.3.1 Reference Clocks (REFCLK400M and FABRIC_CLK)

The fixed reference clocks REFCLK400M and FABRIC_CLK are differential HSTL signals.

REFCLK400M is used as the input clock for the DDR SDRAM interface.

FABRIC_CLK is used as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK400M	400 MHz	IO BANK 67	HSTL	H18	H17
FABRIC_CLK	200 MHz	IO BANK 67	HSTL	H19	G19

Table 5 : DDR REFCLK Connections

3.3.2 Programmable Clocks (PROGCLK0 and PROGCLK1)

There are two programable clock sources that are forwarded throughout the FPGA. These clocks are programmable through the Alpha Data ADA-SDEV-BASE SDK. PROGCLK0 and PROGCLK1 are generated by a dedicated programmable clock generator IC and offer extremely high frequency resolutions (1ppm increments).

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
PROGCLK0[0]	5 - 400 MHz	IO BANK 45	LVDS	AL27	AL28
PROGCLK0[1]	5 - 400 MHz	MGTREFCLK1_224	LVDS	AP10	AP9
PROGCLK0[2]	5 - 400 MHz	MGTREFCLK1_127	LVDS	V32	V33
PROGCLK0[3]	5 - 400 MHz	IO BANK25	LVDS	AN36	AN37

Table 6 : PROGCLK0 Connections

Note: PROGCLK0[3:0] are all buffered copies of the same clock signal. The default (factory set) frequency of PROGCLK0 = 400MHz.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
PROGCLK1[0]	5 - 400 MHz	MGTREFCLK1_225	LVDS	AK10	AK9
PROGCLK1[1]	5 - 400 MHz	IO BANK 64	LVDS	AP19	AP18
PROGCLK1[2]	5 - 400 MHz	IO BANK 48	LVDS	J26	H26
PROGCLK1[3]	5 - 400 MHz	MGTREFCLK1_226	LVDS	AC8	AC7

Table 7 : PROGCLK1 Connections

Note: PROGCLK1[3:0] are all buffered copies of the same clock signal. The default (factory set) frequency of PROGCLK1 = 150MHz.

3.3.3 Module to Carrier Global Clocks (CLK_M2C)

Each connected FMC board can generate a number of differential Global clocks (as per the FMC standard). They each connect to an global clock input on the FPGA.

FMC	Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
1	CLK1_M2C_0	Variable	Bank 44	LVDS	AM22	AN22
1	CLK1_M2C_1	Variable	Bank 44	LVDS	AM21	AN21
2	CLK2_M2C_0	Variable	Bank 24	LVDS	AM32	AN32
2	CLK2_M2C_1	Variable	Bank 24	LVDS	AM31	AN31
2	CLK2_M2C_2	Variable	Bank 64	LVDS	AL19	AL18
2	CLK2_M2C_3	Variable	Bank 64	LVDS	AL17	AM17
3	CLK3_M2C_0	Variable	Bank 46	LVDS	H36	G36
3	CLK3_M2C_1	Variable	Bank 46	LVDS	G37	F37
3	CLK3_M2C_2	Variable	Bank 47	LVDS	F32	E32
3	CLK3_M2C_3	Variable	Bank 47	LVDS	F33	E33

Table 8 : CLK_M2C Connections

3.3.4 Module to Carrier MGTREF Clocks (GBTCLK_M2C)

Each connected FMC board can generate a number of differential MGT Reference clocks (as per the FMC standard). They each connect to an MGTREFCLK input on the FPGA.

FMC	Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
1	GBTCLK1_0_M2C	Variable	MGTREFCLK_225	LVDS	AM10	AM9
2	GBTCLK2_0_M2C	Variable	MGTREFCLK_224	LVDS	AT10	AT9
3	GBTCLK3_0_M2C	Variable	MGTREFCLK_226	LVDS	AH10	AH9
3	GBTCLK3_1_M2C	Variable	MGTREFCLK_227	LVDS	AE8	AE7
3	GBTCLK3_2_M2C	Variable	MGTREFCLK_228	LVDS	AA8	AA7
3	GBTCLK3_3_M2C	Variable	MGTREFCLK_126	LVDS	AD32	AD33
3	GBTCLK3_4_M2C	Variable	MGTREFCLK_127	LVDS	Y32	Y33
3	GBTCLK3_5_M2C	Variable	MGTREFCLK_128	LVDS	T32	T33

Table 9 : GCLK_M2C Connections

3.4 Configuration

There are two main ways of configuring the FPGA on the ADM-SDEV-BASE:

- From Flash memory on the config FMC board, at power-on, as described in Section 3.4.1
- Using a Xilinx Platform JTAG cable connected to the programming header on the config FMC board Section 3.4.2

3.4.1 Configuration From ADM-SDEV-CFG1 or ADM-SDEV-CFG2 Flash Memory

The FPGA can be automatically configured at power-on from two 256 Mbit QSPI flash memory device configured as an x8 SPI device (Micron part numbers MT25QU256ABA8E12-1SIT). These flash devices are typically divided into two regions of 32 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for the FPGA.

It is possible to use Multiboot with a fallback image on this hardware. The master SPI configuration interface and the Fallback MultiBoot are discussed in detail in Xilinx UG570.

The flash address map is as detailed below:

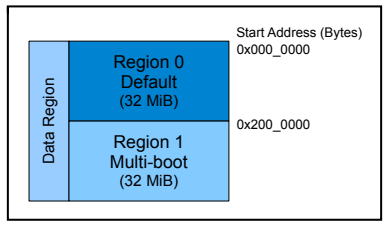

Figure 7 : Flash Address Map

At power-on, the FPGA attempts to configure itself automatically in serial master mode based on the contents of the header in the programing file. See Xilinx UG570 MultiBoot for details.

Note:
If an over-temperature alert is detected from the System Monitor, the FPGA **will be cleared** by pulsing its PROG signal. See Automatic Temperature Monitoring.

3.4.1.1 Building and Programming Configuration Images

Generate a bitfile with these constraints (see xapp1233):

- set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-1} [current_design]
- set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
- set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
- set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]
- set_property BITSTREAM.CONFIG.OVERTEMPSHUTDOWN Enable [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 64
- -interface SPIx8

- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (0th location)
- -loadbit "up 0x2000000 <directory/to/file/filename.bit>" (1st location, optional)

Program with vivado hardware manager with these settings (see xapp1233):

- SPI part: mt25qu256-spi-x1_x2_x4_x8
- State of non-config mem I/O pins: Pull-none
- Target the four files generated from the write_cfgmem tcl command.

3.4.2 Configuration via JTAG

A Xilinx Platform Programming Cable may be attached to the programming header on the Config FMC board. This permits the FPGA to be reconfigured using the Xilinx Vivado Hardware Manager via JTAG. The device will be automatically recognized in Vivado Hardware Manager.

For more detailed instructions, please see “Programming the FPGA Device” section of Xilinx UG908: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_1/ug908-vivado-programming-debugging.pdf

3.5 Health Monitoring

The **ADA-SDEV-BASE** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using the Atmel AVR microcontroller.

Control algorithms within the microcontroller automatically checks line voltages and on board temperatures.

The following voltage rails and temperatures are monitored:

Monitor	Name	*Purpose*	Units
12.0V	ADC00	Board Input Supply	V
5.0V	ADC01	Board Input Supply	V
3.3V	ADC02	Board Input Supply	V
FMC2_VIO	ADC03	Config FMC I/O voltage	V
2.5V	ADC04	Level Translation	V
1.8V	ADC05	FPGA IO Voltage (VCCO)	V
0.95V	ADC06	Target FPGA Core Supply (VccINT)	V
1.8V	ADC07	Target Transceiver Power (AVCC_AUX)	V
1.5V	ADC08	DDR SDRAM, Target FPGA memory I/O	V
1.2V	ADC09	Target Transceiver Power (AVTT)	V
1.0V	ADC10	Target Transceiver Power (AVCC)	V
12.0V Current	ADC11	12V Supply Current Reading	A
5.0V Current	ADC12	5V Supply Current Reading	A
3.3V Current	ADC13	3.3V Supply Current Reading	A
Temp1	TMP00	micrcontroller on-die temperature	deg C
Temp2	TMP01	Board temperature sensor on-die temperature	deg C
Temp3	TMP02	FPGA on-die temperature	deg C

Table 10 : Voltage and Temperature Monitors

Note: The "Name" column contains the name assigned to each sensor in the display-sensors utility report.

3.5.1 Automatic Temperature Monitoring

At power-up, the control logic sets the temperature limits and resets the temperature sensor's over-temperature interrupt.

The temperature limits are shown below :

	FPGA		Board	
	Min	Max	Min	Max
Industrial	-40 degC	+100 degC	-40 degC	+100 degC

Table 11 : Temperature Limits

Important:

If any temperature limit is exceeded, the FPGA is automatically cleared. This is indicated by the Green LED (FPGA Configured) switching off and the two status LEDs showing a temperature fault indication.

The purpose of this mechanism is to protect the card from damage due to over-temperature.

3.5.2 Microcontroller Status LEDs

LEDs D2 (Red) and D1 (Green) indicate the microcontroller status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 12 : Status LED Definitions

3.6 FPGA

3.6.1 I/O Bank Voltages

The FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in Target FPGA IO Banks. Full details of the IOSTANDARD required for each signal are given in the ADA-SDEV-BASE SDK.

IO Banks	Voltage	Purpose
0, 65	FMC2_VIO_B	Configuration, JTAG
44, 45	FMC1_VADJ	LPC FMC GPIO
24, 64	FMC2_VADJ	Config FMC GPIO
25, 46, 47	FMC3_VADJ	FMC+ GPIO
48	FMC3_VIO_B	FMC+ GPIO
66, 67, 68	1.5V	DDR SODIMM

Table 13 : Target FPGA IO Banks

3.6.2 Target MGT Links

There are a total of 32 Multi-Gigabit Transceiver (MGT) links connected to the FPGA:

Links	Width	Connection
FMC1_DP(3:0)	4	links to LPC FMC Socket (J1)
FMC2_DP(3:0)	4	links to Config FMC Socket (J2)
FMC3_DP(23:0)	24	links to FMC+ Socket (J3)

Table 14 : Target MGT Links

Note: link FMC2_DP(1) is unavailable on the CNA1509 package device.

The connections of these links are shown in MGT Links:

For MGT Clocking see Clocks:

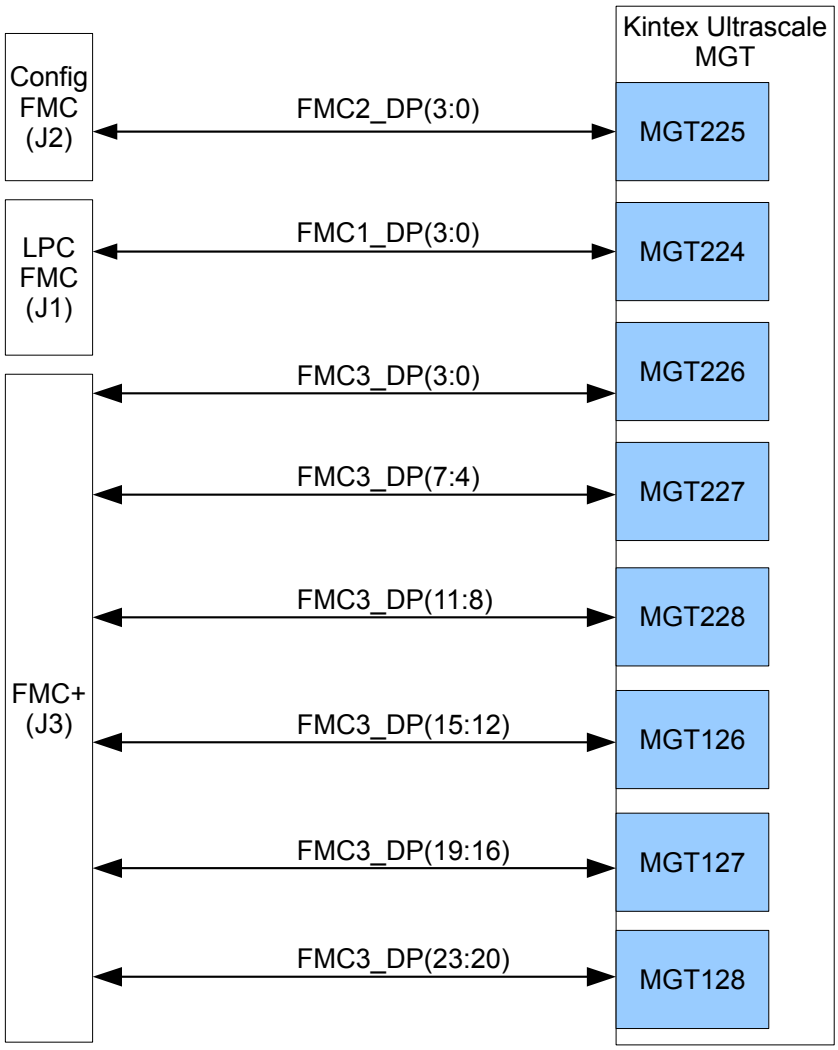

Figure 8 : MGT Links

3.7 Memory Interfaces

The **ADA-SDEV-BASE** has a single SODIMM socket, capable of supporting a DDR3 (with ECC) SODIMM module, spread across 3 FPGA IO banks (66/67/68).

The memory banks are arranged for compatibility with the Xilinx Memory Interface Generator (MIG). DRAM Banks Shows the FPGA banks used. Full details of the interface, signaling standards and an example design are provided in the ADA-SDEV-BASE SDK.

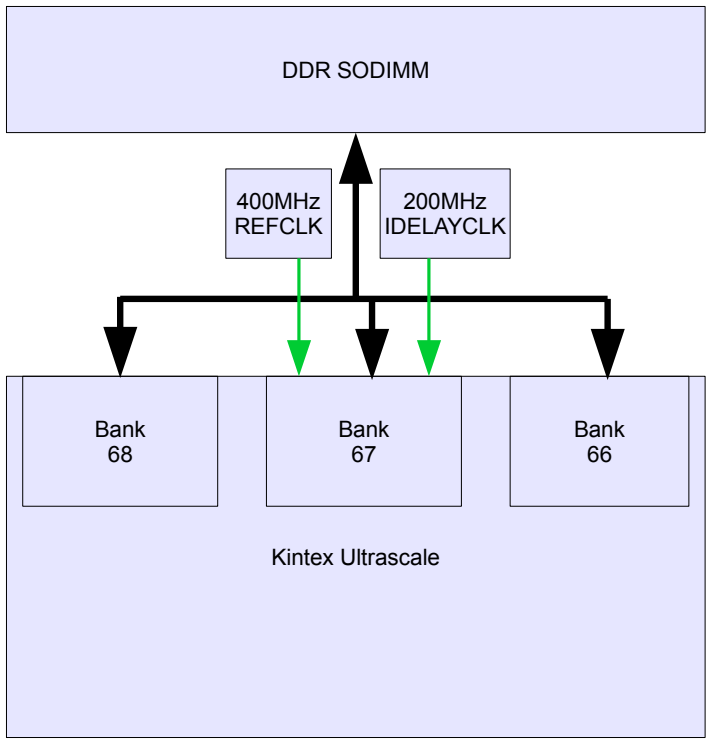

Figure 9 : DRAM Banks

3.8 FMC Interfaces

The **ADA-SDEV-BASE** board has 3 FMC sockets, J1, J2 and J3. Their interfaces are described below.

3.8.1 Low Pin Count (LPC) FMC, J1

Connector J1 is for general purpose IO.

Group	FPGA Bank	Name	Function
FMC1_LA_0	44	FMC1_LA(16:2)	15 diff. Pairs / 30 single-ended
		FMC1_LA_CC (1:0)	2x Regional Clocks / GPIO pairs / 4 single-ended
FMC1_LA_1	45	FMC1_LA(33:19)	15 diff. Pairs / 30 single-ended
		FMC1_LA_CC (18:17)	2x Regional Clocks / GPIO pairs / 4 single-ended

Table 15 : LPC FMC Groups (J1)

3.8.2 Configuration FMC, J2

Connector J2 is used for the FPGA configuration interface plus also for general purpose IO.

Group	FPGA Bank	Name	Function
CONFIG	0,65	Various	FPGA Configuration Interface
FMC2_LA_0	24	FMC2_LA(16:2)	15 diff. Pairs / 30 single-ended
		FMC2_LA_CC (1:0)	2x Regional Clocks / GPIO pairs / 4 single-ended
FMC2_LA_1	64	FMC2_LA(33:19)	15 diff. Pairs / 30 single-ended
		FMC2_LA_CC (18:17)	2x Regional Clocks / GPIO pairs / 4 single-ended

Table 16 : Config FMC Groups (J2)

3.8.3 High Pin Count FMC+, J3

Connector J3 is used for general purpose IO.

Group	FPGA Bank	Name	Function
FMC3_LA_0	46	FMC3_LA(16:2)	15 diff. Pairs / 30 single-ended
		FMC3_LA_CC (1:0)	2x Regional Clocks / GPIO pairs / 4 single-ended
FMC3_LA_1	47	FMC3_LA(33:19)	15 diff. Pairs / 30 single-ended
		FMC3_LA_CC (18:17)	2x Regional Clocks / GPIO pairs / 4 single-ended
FMC3_HA_0	25,46	FMC3_HA(16:2)	15 diff. Pairs / 30 single-ended
		FMC3_HA_CC (1:0)	2x Regional Clocks / GPIO pairs / 4 single-ended
		FMC3_HA(23:18)	6 diff. Pairs / 12 single-ended
		FMC3_HA_CC (17)	Regional Clock / GPIO pair / 2 single-ended
FMC3_HB_0	48	FMC3_HB(5:1)	5 diff. Pairs / 10 single-ended

Table 17 : FMC+ Groups (J3) (continued on next page)

Group	FPGA Bank	Name	Function
FMC3_HB_0	48	FMC3_HB(16:7)	10 diff. Pairs / 20 single-ended
		FMC3_HB(21:18)	4 diff. Pairs / 8 single-ended
		FMC3_HB_CC (0)	Regional Clock / GPIO pair / 2 single-ended
		FMC3_HB_CC (6)	Regional Clock / GPIO pair / 2 single-ended
		FMC3_HB_CC (17)	Regional Clock / GPIO pair / 2 single-ended

Table 17 : FMC+ Groups (J3)

3.8.4 FMC VADJ Power Supplies

The ADM-SDEV-BASE/XCKU060 board is fully compliant with the VITA 57.1 standard. This means that any FMC card that is used with the board should have an EEPROM on board programmed according to the IPMI format defined in the VITA 57.1 FMC specification.

The IPMI specification notes that an FMC board should use a 2K EEPROM which is compatible with 24C02 devices. This EEPROM must be available to be queried at power on in order that the FMC slot VADJ voltage can then be set up and turned on.

If this specification is not followed, the VADJ voltage to the FMC slot in question will not automatically power up (it will correctly remain at 0V).

Note:
In the event that this EEPROM is not present on the FMC board, an alternative method of configuring the FMC VADJ power supply is also possible. The use of this alternative method is not recommended practice. Please contact Alpha Data support for further details if required.

Appendix A: Rev1 PCB Top View

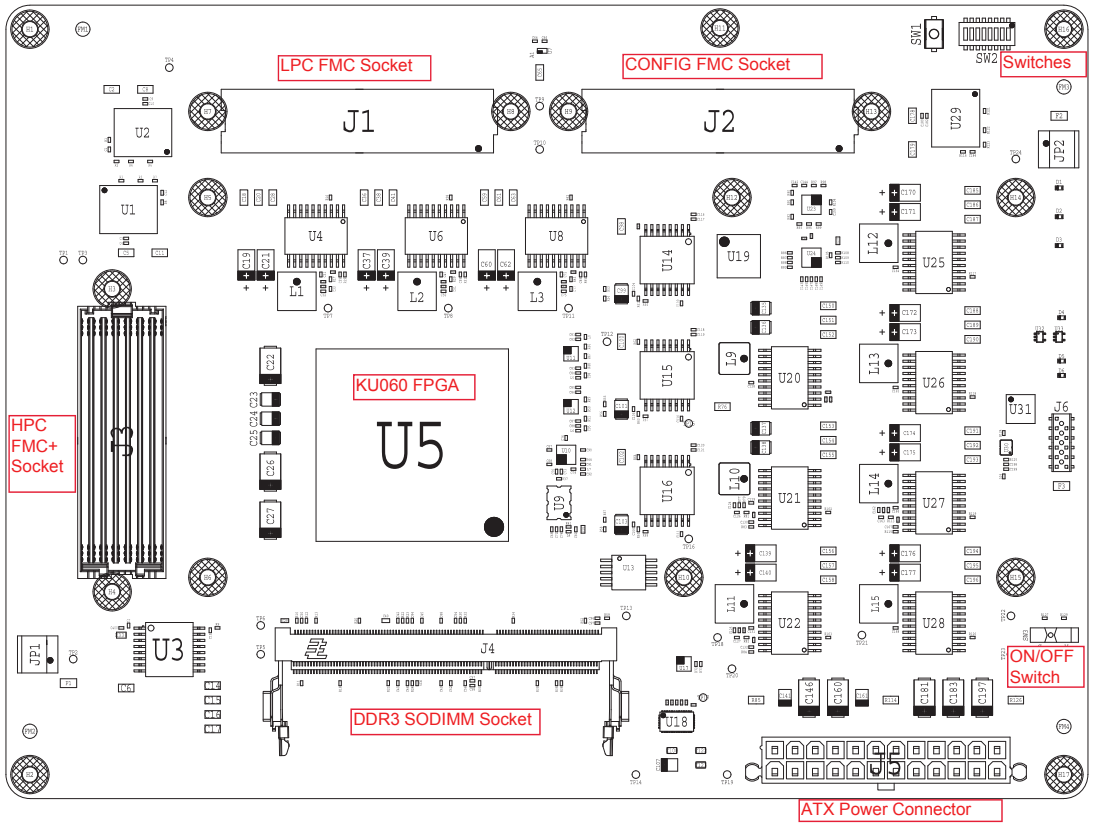

Figure 10 : ADM-SDEV-BASE/XCKU060 Top View (rev1 board shown)

Revision History

Date	Revision	Nature of Change
12 Sep 2018	0.1	Initial Draft
21 Sep 2018	0.2	Updated after review
27 Nov 2018	1.0	First Release
28 Aug 2019	1.1	Updated sensor table to include sensor name
23 Sep 2019	1.2	Updated references table and section on ATX power supply
11 Oct 2019	1.3	Corrected error in release date of previous version
29 Feb 2020	1.4	Added mention of new user LEDs on Rev 2 pcb
18 May 2020	1.5	Added definition of differences between rev1 and rev2 pcbs
19 May 2020	1.6	Added section regarding turn on of FMC ADJ power supplies.
27 Apr 2021	1.7	Amended any references to CFG1 board to include CFG2.

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